

Modified gain boosting charge pump for low current mismatch and high performance phase-lock loop

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Abstract

In conventional CMOS charge pump circuits there are some current mismatching characteristics which result in a phase offset in phase-locked loop circuits. This paper presents a new charge pump circuit after scrutinizing the deeper examination of the existing current mismatch problem. It combines an error amplifier with reference current sources to achieve good current matching characteristics and lower phase noises, and at the same time it can eliminate charge sharing by using charge removal transistors. In addition to gain-boosting, used to increase the output impedance of the CP, a low-voltage cascode current mirror is used to enhance current matching over process corners. A good matching of the CP is achieved with current mismatch equals to 0.6% in typical conditions and 1% over all process variations. The CP output compliance voltage range of

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0.1-1.8 V is achieved for 1.8-V supply voltage. The circuit was designed using 0.18 μ m TSMC CMOS technology and simulated by Spectre tools.

Keywords: Charge pump (CP), gain-boosting charge pump, low-voltage cascode current mirror, phase-locked loop (PLL).

1 Introduction

Since the conception of phase locking was proposed in the Thirties of the 20th Century, it has been widely applied in electronics and communication fields [5], especially used in large scale digital circuits. CP-PLLs (Charge Pump Phase-Locked Loop) are mainly used to generate signals and renew the clock pulses during the data transmission with high speed [3], [4]. As a key model, the charge pump plays an important role in assuring PLLs stability. It converts the digital signals in PFDs (Phase Frequency Detector) into analog signals of VCOs (Voltage Controlled Oscillator). When the phase-locked loop was locked in a certain frequency, the output voltage of charge pump is demanded to be a fixed value, and any tiny change of which will result in apparent frequency offset. Therefore, it is very important to design a charge pump circuit which can send a stable output voltage in CP-PLLs plan.

Phase-locked loops are widely used in clock generators and RF transceivers to ensure the accuracy of the oscillator frequency. The charge pump (CP) is an essential block in phase-locked loops (PLL). The CP consists of two switched current sources. Any current mismatch between the two current sources (i.e., difference between the source and the sink currents) would cause ripples on the control voltage. Ripples result in large phase noise and would also cause spurs on the PLL output signal [6].

This paper proposes a modified technique to decrease current mismatch in

CP's using gain-boosting in addition to low-voltage cascode current mirrors [5]. Section 2 reviews the basic idea of the CP and the reasons behind current mismatch. Section 3 introduces the proposed circuit architecture. Finally simulation results and comparisons in section 4. Section 5 concludes the paper.

2 Basic principle

Figure 1 shows the circuit diagram of a conventional charge pump. In the charge pump, the digital output signals (UP and DN) of the PFD control the two circuit sources (I_{UP} and I_{DN}), and charge the capacitance C_L via two switches which generally substituted by two MOSFET to obtain the DC level V_{ctrl} needed by the Voltage Controlled Oscillator.

In Figure 1 the I_{UP} and I_{DN} should be completely equal in theory, but there are many nonideal effects which will result in their mismatching in practice [1].

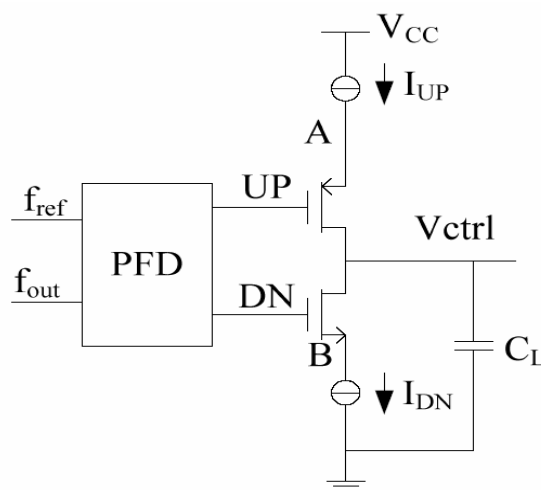


Figure 1: Conventional charge pump schematic

Another ubiquitous problem is the charge sharing in conventional charge pumps which results from the parasitic capacitance of node A and B. The level in node A will be charged to VDD, and in node B be discharged to GND when the signal UP and DN are invalid, whereas the node A level will be falling and the node B level will be rising when the signal UP and DN are valid. The difference between V_{ctrl} and node A will not be uniform to the difference between V_{ctrl} and node B, thus bring on the charge redistribution among CL, A and B. Because the I_{ds} will change with V_{ds} , current source I_{UP} or I_{DN} will share the charge. It will result in current mismatch which make V_{ctrl} jittering, and influence the circuit performance. The output V_{ctrl} would be held if the charge and discharge current are well matched. Generally, the net current generated by the charge pump is not equal to zero because of the current mismatching, it will make the V_{ctrl} increase a fixed value in every phase comparing time. The control voltage V_{ctrl} should be held in an average value to maintain the loop in a locked status (as shown in Figure 2), then the phase-locked loop shall bring on phase error which make the net current of the charge pump be zero in every period, as shown in Figure 3 where A1 and A2 have the equal area.

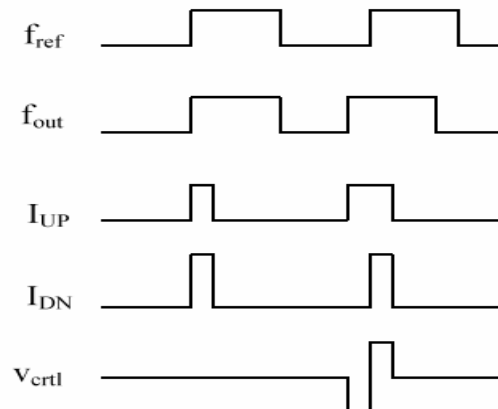


Figure 2: Charge and discharge current mismatch

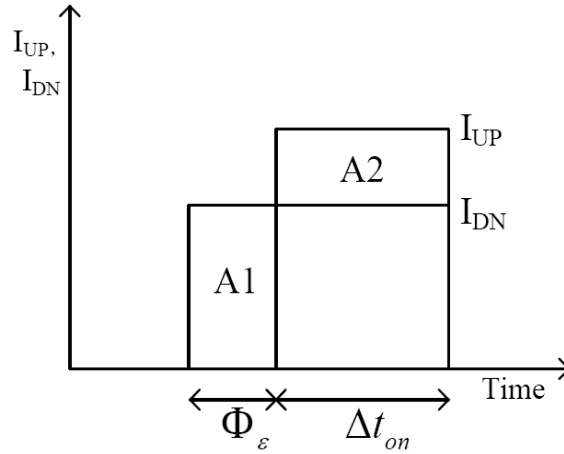


Figure 3: Conventional charge pump current mismatch

The phase error resulted from the current mismatch can be expressed as the following formula where Δt_{on} , I_{CP} and $|I_{UP} - I_{DN}|$ respectively represent the dead zone time of the PFD, the period of the reference clock, and the offset between CP current and charge, discharge current.

$$\phi_{\epsilon} = 2\pi \cdot \frac{\Delta t_{on}}{T_{ref}} \cdot \frac{|I_{UP} - I_{DN}|}{I_{CP}} \quad (1)$$

The equation (1) indicates that, to lower the phase error, the dead zone time Δt_{on} and mismatch current $|I_{UP} - I_{DN}|$ should be reduced, but the CP current I_{CP} should be increased while the reference clock period is fixed. Holding a definite dead zone time will be propitious to overcoming the PFD dead zone, and the higher current I_{CP} will increase the power consumption and noise, so lessening the mismatch current $|I_{UP} - I_{DN}|$ is the key to lower the CP phase error.

To solve this problem, a novel charge pump circuit which use error amplifier and reference current source is proposed to obtain the improved characteristic for current match, and reduce the PLL's phase noise. Simultaneously, the charge sharing is effectively restrained by using charge

removal transistors. So the circuit possesses good current match and high working speed. Current mirrors are then used to copy currents from the bias cell, and a cascode is used at the output node to get high output impedance in order to reduce current mismatch.

Gain-boosting technique is applied shown in Figure 4, high output impedance can be achieved without adding more cascode devices [5]. Gain-boosting saves some voltage headroom; this is significant for short channel length technologies with low supply voltage.

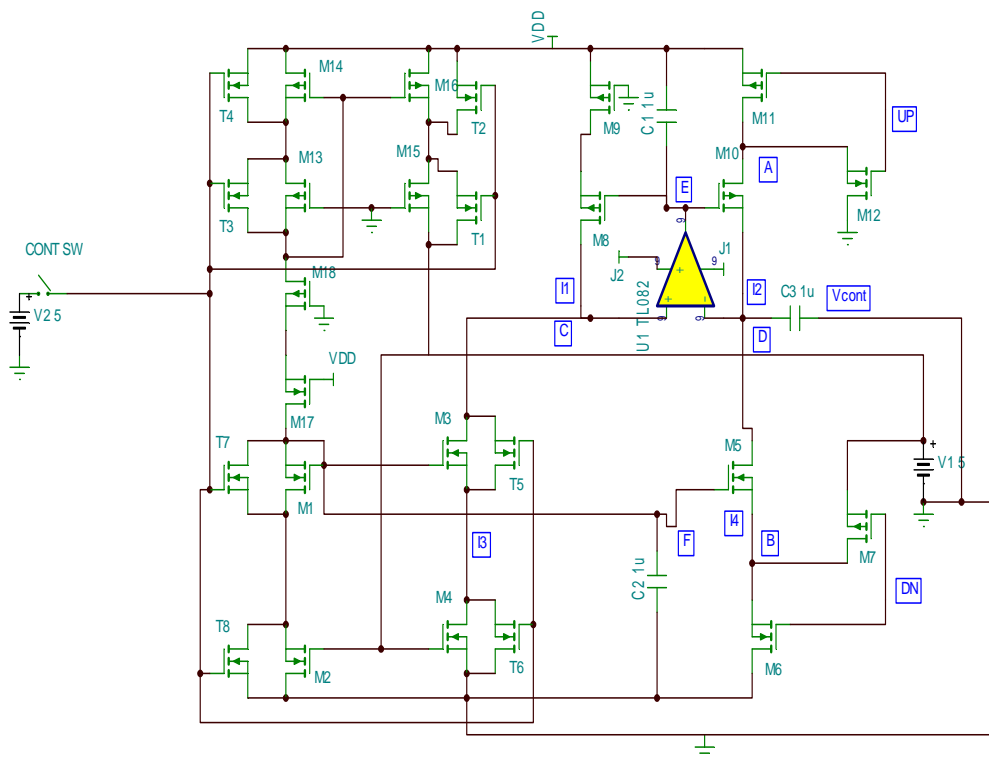


Figure 4: Proposed charge Pump

3 Proposed circuit

The proposed CP circuit greatly improves the circuit performance by enhancing the current match and lessening the charge sharing, and at the same time, possessed the characteristics of high operating speed and low power consumption. In Figure 4, capacitance C1, C2 fill the role of stabilizing the node E and F's voltage to avoid instantaneous grid voltage fluctuation of the current source. The voltage V_c in node C will change with V_{ctrl} by inserting an error amplifier which has the gain high enough to make V_c equal V_{ctrl} . Moreover, M11 is designed to equal M9, M8 equal M10, M3 equal M5, and M4 equal M6, so the current I_4 will be the same as I_3 , I_1 when UP, DN level is holding high, and I_2 will be the same as I_1 , I_3 when UP, DN level is holding low.

Finally the current I_4 equals I_2 , which lead up to the result of almost perfect drain-source current matching. M7 and M12 are named as charge eliminating transistor. When the transistors transfer from saturation to cutoff, the charge resting on the channel will be emitted to the source, and that the drain will not be impacted. When the UP and DN is low, the spare charge will be removed from node A and B, so that the charge sharing can be successfully restrained.

The proposed CP circuit which use error amplifier and reference current source to get good match characteristic, and use charge removal transistor to restrain the charge sharing. All the design has been simulated with Spectre tools.

The shortcoming of the structure is that it will confine the dynamic range, but it is not important in most situations. While V_{ctrl} less than $V_{g5} - V_{tn}$ and DN invalid, the current will move to the output via M7. The V_{ctrl} will not be less than V_{tn} during NMOS used as VCO current control, and forcing the V_{g5} less than $2V_{tn}$ will be easy to implement. Because the V_{ctrl} is up to $V_{g10} + |V_{tp}|$, it restricts the V_{ctrl} range. Transistor M7 and M12 also improve the switch speed of current, and supply DC level for node A, B while switch is turned off, which will prevent the pending nodes influencing the control Voltage.

A modification for the gain-boosting CP is illustrated in Figure 4, in which

the channel length modulation problem is solved as well as current mismatch. A low voltage cascode current mirror is used to copy I_{UP} and I_{Down} from a single current source to ensure that both currents are equal.

Figure 4 shows the low-voltage cascode current mirror. This current mirror is chosen because it provides high output impedance, and low channel length modulation mismatch [5].

As shown in Figure 4, the UpB and Down controlled switches have been embedded in the low-voltage cascode current mirrors, where M7 and M8 are the UpB and Down controlled switches respectively, M9 to M16 are the low voltage cascode current mirror transistors, and finally M17 and M18 are the reference current generators. The bias voltage of the low-voltage cascode current mirrors is chosen to be GND for the PMOS switched mirror, and VDD for the NMOS switched mirror, as these are the values of UpB and Down signals at lock. This provides better matching.

The output impedance, R_{out} , is higher than that given in (2), since there is another cascode transistor, R_{out} is given by

$$R_{out} = r_{06} \cdot g_{m5} \cdot r_{05} \quad (2)$$

at the node D. This value is large, and so large length transistors are not needed for having high output impedance.

4 Simulation results

The proposed charge pump circuit, at the 1.8V power source, is simulated with Spectre tools. Figure 5 shows the simulation result of CP charge circuit, and Figure 6 shows the CP Charging node voltage.

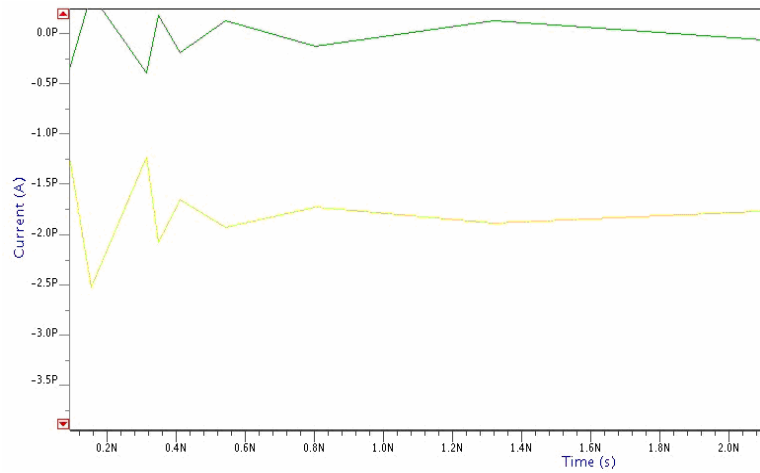


Figure 5: IUp and IDown currents Plots

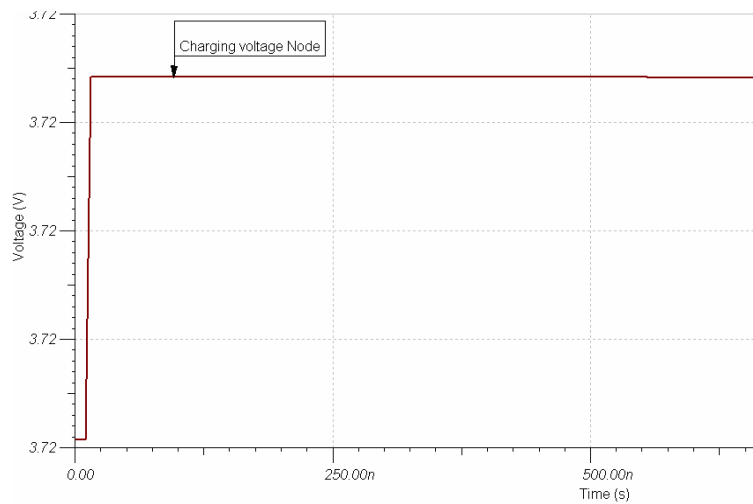


Figure 6: Charging voltage Node

In the diagram the V_{ctrl} ascends linearly without sunken or bulgy undulation, and the simulation graph accords with the requirement. Figure 7 represents the relationship of discharge voltage node.

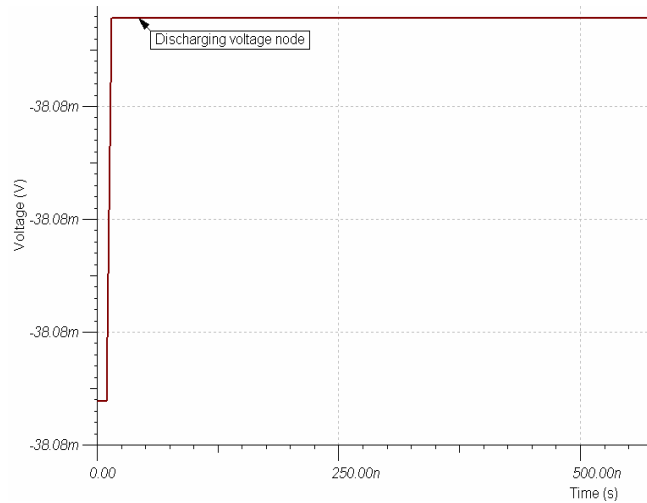


Figure 7: Discharging voltage Node

The proposed modified gain-boosting CP is designed using 1.8V CMOS transistors, good current matching is observed in addition to a wide compliance voltage range of 0.1-1.7 V, which relaxes the VCO design. The maximum value for the current mismatch is less than 1%.

Table 1: Current mismatch results

<i>Proposed Charge Pump</i>		<i>Gain Boosting CP</i>	
$I_p(\mu\text{A})$	Mismatch(%)	$I_p(\mu\text{A})$	Mismatch(%)
16.23	0.61	14.5	0.8

5 Conclusion

By using the gain-boosting and low-voltage cascade current mirrors, a high-performance low-mismatch charge pump is achieved. Mismatch between the two current sources of the CP is 0.6% for typical Conditions and 1% over all process variations. Moreover, a very wide output compliance voltage range is obtained for 1.8-V supply using 180-nm technology.

References

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